(19)日本国特許庁（ＪＰ）　(12)**公開特許公報（Ａ）**　(11)特許出願公開番号
特開2000－250480
（P2000－250480A）
(43)公開日　平成12年９月14日(2000.9.14)

(51)Int.Cl.[7]	識別記号	ＦＩ		テーマコード（参考）
Ｇ０９Ｇ　3/28		Ｇ０９Ｇ　3/28	Ｋ	
3/20	６４１	3/20	６４１Ｅ	

審査請求　未請求　請求項の数２　ＯＬ　（全 6 頁）

(21)出願番号　特願2000－40919(P2000－40919)

(22)出願日　平成12年２月18日(2000.2.18)

(31)優先権主張番号　１９９９－６６４０

(32)優先日　平成11年２月27日(1999.2.27)

(33)優先権主張国　韓国（ＫＲ）

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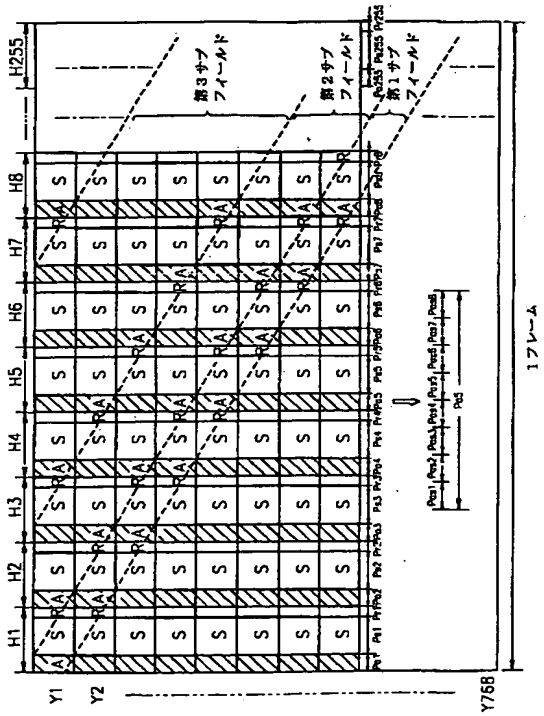
(54)【発明の名称】　プラズマ表示パネルの駆動方法

(57)【要約】　（修正有）
【課題】　駆動装置を単純に、設計、変更を容易に、輝度を高くする。
【解決手段】　単位フレームを階調の数に相応する個数の単位駆動周期Ｈ１～Ｈ２５５に分割し、各単位駆動周期を単位アドレス周期、単位維持放電周期及び単位リセット周期に三分し、各単位アドレス周期をｐ個の時間に分割し各サブフィールドに割り当てる。各サブフィールドは各走査電極ラインＹ１～Ｙ７６８に対して単位駆動周期の時間差を有して順次に始まりながら相互重畳される。各割り当てた時間では、サブフィールドの最初の単位駆動周期に相応する走査電極ラインとアドレス電極ラインとの間にアドレス電圧を印加し、全ての単位維持放電周期では共通電極ラインと全ての走査電極ラインとの間に維持放電電圧を印加し、各単位リセット周期では、共通電極ラインと、サブフィールドの最終の単位駆動周期に相応する走査電極ラインの間にリセット電圧を印加する。



維持放電周期とが分離される駆動方法である。これにより、駆動装置の設計及び変更が容易で駆動装置が単純になる利点がある。しかし、維持放電周期が相対的に短くなって表示輝度が低くなるという問題点を有する。

【００１１】一方、表示中アドレス駆動方法は各サブフィールドの表示周期内にアドレス周期が含まれ、各サブフィールドが各走査電極ラインに対して単位時間差を有して順次に始まりながら相互重畳される駆動方法である。これにより、維持放電周期が相対的に延びて表示輝度が高くなる利点がある。しかし、駆動装置の設計及び変更が難しく、駆動装置が複雑になるという問題点がある。

【００１２】

【発明が解決しようとする課題】本発明の目的は、駆動装置の設計及び変更が容易になり、駆動装置が単純になり、表示輝度も高くなるプラズマ表示パネルの駆動方法を提供することにある。

【００１３】

【課題を解決するための手段】前記目的を達成するための本発明の駆動方法は、相互対向離隔された前面基板と背面基板とを有し、前記前面及び背面基板の間に共通電極ライン、走査電極ライン及びアドレス電極ラインが整列され、前記共通電極ラインと走査電極ラインとが相互並んで整列され、前記アドレス電極ラインが前記走査電極ラインに対して直交に整列され、各交差点に相応する画素が規定されたプラズマ表示パネルの単位フレームに、各々アドレス段階、維持放電段階及びリセット段階が遂行されるｐ個のサブフィールドで階調表示を遂行するための駆動方法である。

【００１４】この方法は、表示される単位フレームを階調の数に相応する個数の単位駆動周期に分割する段階を含む。前記各単位駆動周期は単位アドレス周期、単位維持放電周期及び単位リセット周期に三分され、各単位アドレス周期が相互同じ、各単位維持放電周期も相互同じ、各単位リセット周期も相互同じである。前記各単位アドレス周期はp個の時間に分割され、分割された各サブフィールドに割り当てられる。前記各サブフィールドは前記各走査電極ラインに対して前記単位駆動周期の時間差を有して順次に始まりながら相互重畳される。前記各単位アドレス周期内の各割り当てられた時間では、サブフィールドの最初の単位駆動周期に相応する走査電極ラインとアドレス電極ラインとの間にアドレス電圧が印加される。前記全ての単位維持放電周期では共通電極ラインと全ての走査電極ラインとの間に維持放電電圧が印加される。前記各単位リセット周期では、前記共通電極ラインと、サブフィールドの最終の単位駆動周期に相応する走査電極ラインの間にリセット電圧が印加される。

【００１５】前記全ての単位維持放電周期で共通電極ラインと全ての走査電極ラインとの間に維持放電電圧が印加されても、その直前のアドレス周期に選択されて壁電荷が形成された画素のみは維持放電が遂行できる。

【００１６】前述したように、本発明の駆動方法によると、前記各単位駆動周期により駆動され、前記全ての単位維持放電周期では共通電極ラインと全ての走査電極ラインとの間に維持放電電圧が印加される。これにより、駆動装置の設計及び変更が容易になり、駆動装置が単純になり得る。又、前記各サブフィールドは前記各走査電極ラインに対して前記単位駆動周期の時間差を有して順次に始まりながら相互重畳される。これにより、単位フレーム内で維持放電周期が相対的に延びて表示輝度が高くなる。

【００１７】

【発明の実施の形態】以下、添付した図面を参照して本発明の望ましい実施の形態を詳細に説明する。

【００１８】図１は本発明の一実施の形態の駆動方法を説明するための単位フレームの構造を示す。図１の駆動方法は、前面及び背面基板4, 13の間に768本の共通電極ライン(X1, …, X768)、768本の走査電極ライン(Y1, …, Y768)及びアドレス電極ライン(A1, …, Am)が整列され、共通電極ライン(X1, …, X768)と走査電極ライン(Y1, …, Y768)とが相互並んで整列され、アドレス電極ライン(A1, …, Am)が走査電極ライン(Y1, …, Y768)に対して直交に整列され、各交差点に相応する画素が規定されたプラズマ表示パネルに適用される。又、単位フレーム上で各々アドレス段階、維持放電段階及びリセット段階が遂行される８個のサブフィールドにより256階調表示を遂行するための駆動方法である。

【００１９】図１を参照すれば、表示される単位フレームは階調の数より一つ少ない255個の単位駆動周期(H1, …, H255)に分割される。各単位駆動周期(H1, …, H255)は単位アドレス周期(Pa1, …, Pa255)、単位維持放電周期(Ps1, …, Ps255)及び単位リセット周期(Pr1, …, Pr255)に三分される。ここで、各単位アドレス周期(Pa1, …, Pa255)が相互同じ、各単位維持放電周期(Ps1, …, Ps255)も相互同じ、各単位リセット周期(Pr1, …, Pr255)も相互同じである。

【００２０】各サブフィールドは各走査電極ライン(Y1, …, Y768)に対して単位駆動周期(H1, …, H255)の時間差を有して順次に始まりながら相互重畳される。各サブフィールドの開始時点から終了時点までの時間は一つのフレームを占めるが、各サブフィールドがいずれの時点でも全て重畳されるので、一つのフレームに全てのサブフィールドが含められる結果を有する。第１サブフィールドは、ｎ番目走査電極ラインに対してｎ番目単位駆動周期を含む。第２サブフィールドは、ｎ番目走査電極ラインに対してｎ+１番目及びｎ+２番目単位駆動周期を含む。第３サブフィールドはｎ番目走査電極ラインに対してｎ+３番目から及びｎ+６番目単位駆動周期を含む。第４サブフィールドはｎ番目走査電極ラインに対してｎ+７番目から及びｎ+14番目単位駆動周期を含む。第５サブフ

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ィールドはｎ番目走査電極ラインに対してｎ+15番目から及びｎ+30番目単位駆動周期を含む。第６サブフィールドはｎ番目走査電極ラインに対してｎ+31番目から及びｎ+62番目単位駆動周期を含む。第７サブフィールドはｎ番目走査電極ラインに対してｎ+63番目から及びｎ+126番目単位駆動周期を含む。そして、第８サブフィールドはｎ番目走査電極ラインに対してｎ+127番目から及びｎ+254番目単位駆動周期を含む。これにより、256階調表示が遂行できる。

【００２１】各単位アドレス周期(Pa1, …, Pa255)はサブフィールドの数に相応する８個の時間(Pas1, …, Pas8)に分割され、分割された各時間(Pas1, …, Pas8)は各サブフィールドに割り当てられる。各単位アドレス周期(Pa1, …, Pa255)の第１時間(Pas1)は第１サブフィールドに、第２時間(Pas2)は第２サブフィールドに、第３時間(Pas3)は第３サブフィールドに、第４時間(Pas4)は第４サブフィールドに、第５時間(Pas5)は第５サブフィールドに、第６時間(Pas6)は第６サブフィールドに、第７時間(Pas7)は第７サブフィールドに、第８時間(Pas8)は第８サブフィールドに各々割り当てられる。このように各単位アドレス周期(Pa1, …, Pa255)が分割及び割り当てられる理由は、各サブフィールドがいずれの時点でも全て重畳されるからである。即ち、相異なる時点でアドレッシングを遂行して各時点毎に一つの画素のみをアドレッシングするためである。

【００２２】各単位アドレス周期(Pa1, …, Pa255)内の各割り当てられた時間では、サブフィールドの最初の単位駆動周期に相応する走査電極ライン(Y1, …, Y768の中でいずれか一つ)とアドレス電極ライン(A1, …, Amの中でいずれか一つ)との間にアドレス電圧が印加される。全ての単位維持放電周期(Ps1, …, Ps255)では共通電極ライン(X1, …, X768)と全ての走査電極ライン(Y1, …, Y768)との間に維持放電電圧が印加される。即ち、共通電極ライン(X1, …, X768)と全ての走査電極ライン(Y1, …, Y768)とに複数のパルスが交互に印加される。各単位リセット周期(Pr1, …, Pr255)では、共通電極ライン(X1, …, X768)と、サブフィールドの最終の単位駆動周期に相応する走査電極ライン(Y1, …, Y768の中でサブフィールドの数の８本のライン)の間にリセット電圧が印加される。

【００２３】例えば、第１及び第２駆動周期(H1, H2)での駆動過程を説明すると次の通りである。

【００２４】第１単位アドレス周期(Pa1)内の第１時間(Pas1)では第１走査電極ライン(Y1)と、相応するアドレス電極ライン(A1, …, Amの中でいずれか一つ)の間にアドレス電圧が印加され、表示される画素で壁電荷が生成される。第１単位維持放電周期(Ps1)では共通電極ライン(X1, …, X768)と全ての走査電極ライン(Y1, …, Y768)との間に維持放電電圧が印加される。これにより表示される画素で維持放電が遂行される。第１単位リセット周期(Pr1)では、共通電極ライン(X1, …, X768)と、サブフィー

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ルドの最終の単位駆動周期に相応する８本の走査電極ライン(Y1, Y2, …)の間にリセット電圧が印加される。これにより、サブフィールドの最終時点に相応する画素でリセット放電が遂行される。

【００２５】第２単位アドレス周期(Pas2)内の第１時間(Pas1)では第１走査電極ライン(Y1)と、相応するアドレス電極ライン(A1, …, Amの中でいずれか一つ)の間にアドレス電圧が印加され、表示される画素で壁電荷が生成される。第２単位アドレス周期(Pa2)内の第２時間(Pas2)では第１走査電極ライン(Y2)と、相応するアドレス電極ライン(A1, …, Amの中でいずれか一つ)の間にアドレス電圧が印加され、表示される画素で壁電荷が生成される。第２単位維持放電周期(Ps2)では共通電極ライン(X1, …, X768)と全ての走査電極ライン(Y1, …, Y768)との間に維持放電電圧が印加される。これにより表示される画素で維持放電が遂行される。第２単位リセット周期(Pr2)では、共通電極ライン(X1, …, X768)と、サブフィールドの最終の単位駆動周期に相応する８本の走査電極ライン(Y2, Y3, …)の間にリセット電圧が印加される。これにより、サブフィールドの最終時点に相応する画素でリセット放電が遂行される。

【００２６】

【発明の効果】前述したように、本発明に係るプラズマ表示パネルの駆動方法によると、各単位駆動周期(H1, …, H255)により駆動され、全ての単位維持放電周期(Ps1, …, Ps255)には共通電極ライン(X1, …, X768)と全ての走査電極ライン(Y1, …, Y768)との間に維持放電電圧が交互に印加される。これにより、駆動装置の設計及び変更が容易になり、駆動装置が単純になり得る。又、各サブフィールドは各走査電極ライン(Y1, …, Y768)に対して単位駆動周期(H1, …, H255)の時間差を有して順次に始まりながら相互重畳される。これにより、単位フレーム内で維持放電周期(Ps1+Ps2+…+Ps255)が相対的に延びて表示輝度が高くなり得る。

【００２７】本発明は、前記実施の形態に限らずに、特許請求の範囲で定義された発明の思想及び範囲内で当業者により変形及び改良できる。

【図面の簡単な説明】

【図１】本発明の一実施の形態の駆動方法を説明するための単位フレームの構造図である。

【図２】一般的なプラズマ表示パネルの構造を示す図面である。

【図３】図２のプラズマ表示パネルの電極ラインパターン図である。

【図４】図２のパネルの一つの画素のさらに他の例を示す断面図である。

【符号の説明】

1　表示パネル

10, 13　ガラス基板

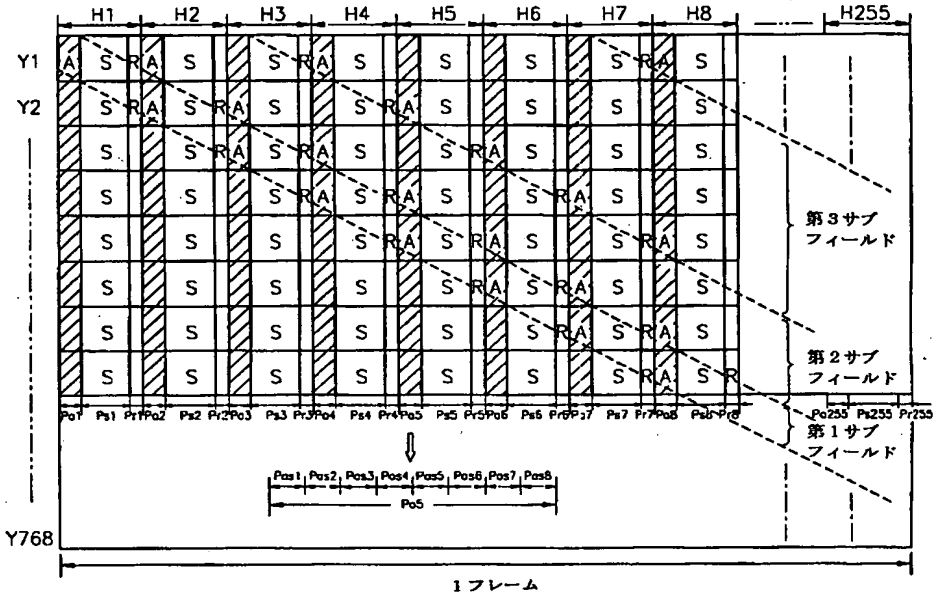
11, 141　誘電体層

12 一酸化マグネシウム層

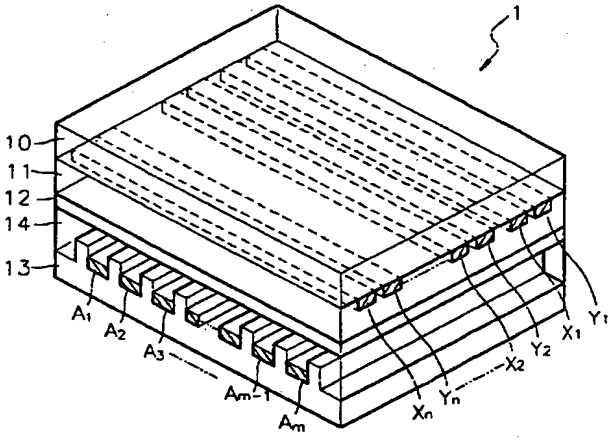
14 放電空間

142 蛍光体

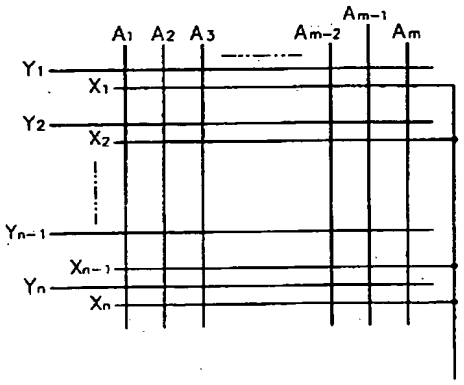
【図１】



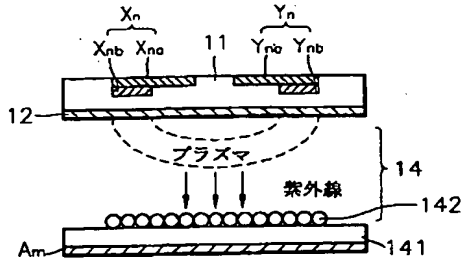
【図２】



【図３】



【図４】



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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-250480

(43)Date of publication of application : 14.09.2000

(51)Int.CI. G09G 3/28

G09G 3/20

(21)Application number : 2000-040919

(22)Date of filing : 18.02.2000

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(30)Priority

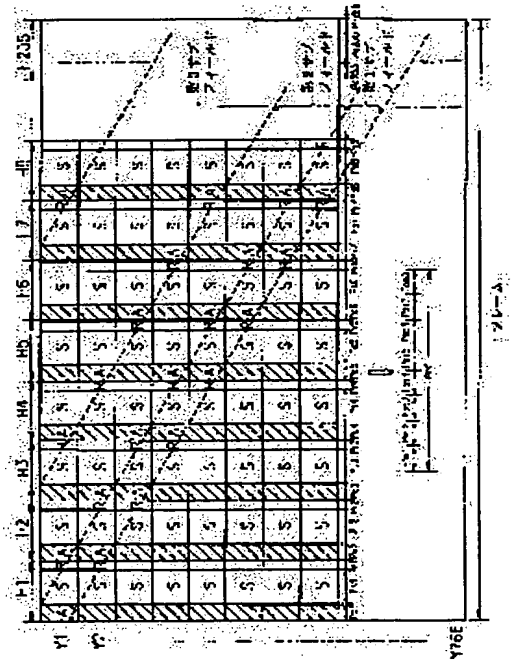
Priority number : 99 9906640 Priority date : 27.02.1999 Priority country : KR

(54) DRIVING METHOD FOR PLASMA DISPLAY PANEL

(57)Abstract:

PROBLEM TO BE SOLVED: To make the constitution of a device simple, to make the desiging and the changing of the device easier and to make the luminance of the display of the device higher.

SOLUTION: A unit frame is divided into unit driving periods H1 to H255 of the number corresponding to the number of gradations and each unit driving period is trisected into an unit address period, an unit sustaining discharge period and an unit reset period and each unit address period is diviced into (p) pieces of times and these times are assigned to respective subfields. Respective subfields are mutually piled up while being made to have the time difference of the unit driving period with respect to respective scan electrode lines Y1 to Y768 and being made to being successively. In each assigned time, an address voltage is applied between a scan electrode line and an address electrode line corresponding to the first unit driving period of a subfield and in all unit sustaining discharge periods, a sustaining discharge voltage is applied among a common electrode line and all scan electrode lines and in each unit reset period, a reset voltage is applied between the common electrode line and a scan electrode line corresponding to the last unit driving period of the subfield.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

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CLAIMS

[Claim(s)]
[Claim 1] It has the front substrate and tooth-back substrate which are characterized by providing the following and by which mutual opposite isolation was carried out. A common electrode line, a scanning electrode line, and an address electrode line align between the aforementioned front substrate and a tooth-back substrate. On the unit frame of the plasma display panel as which the pixel which the aforementioned common electrode line and a scanning electrode line align by mutual ****, and the aforementioned address electrode line aligns to the aforementioned scanning electrode line at a rectangular cross, and ****s in each crossing was specified The drive method for carrying out a gradation display by two or more subfields by which an address stage, a maintenance electric discharge stage, and a reset stage are carried out respectively The stage of dividing the unit frame displayed into the unit drive period of the number which ****s in the number of gradation each aforementioned unit drive period -- a unit address period, a unit maintenance electric discharge period, and a unit reset period -- dividing into three -- each unit address period -- mutual -- the same -- each unit maintenance electric discharge period -- mutual -- the same -- each unit reset period -- mutual -- the stage made the same The stage which divides each aforementioned unit address period at the time of the number of the aforementioned subfield, and assigns each divided time to each subfield Mutual superposition is carried out, while each aforementioned subfield has the time difference of the aforementioned unit drive period to each aforementioned scanning electrode line and starts one by one. in each quota **** time in each aforementioned unit address period The stage of impressing address voltage between the scanning electrode lines and address electrode lines which **** to the unit drive period of the beginning of a subfield, The stage of impressing maintenance discharge voltage between a common electrode line and all scanning electrode lines the unit maintenance electric discharge period of all above, and each aforementioned unit reset period The stage of impressing reset voltage between the aforementioned common electrode line and the scanning electrode line which ****s to the last unit drive period of a subfield
[Claim 2] The drive method of the plasma display panel according to claim 1 characterized by impressing two or more pulses to the aforementioned common electrode line and all scanning electrode lines by turns in the stage of impressing the aforementioned maintenance discharge voltage.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the drive method of a plasma display panel, and relates to the drive method of the plasma display panel for carrying out a gradation display on a unit frame by two or more subfields by which an address stage, a maintenance electric discharge stage, and a reset stage are carried out in more detail respectively.
[0002]
[Description of the Prior Art] Drawing 2 shows the structure of a general plasma display panel. Drawing 3 shows the electrode line pattern of the plasma display panel of drawing 2 . Drawing 4 shows the 1-pixel example of the panel in drawing 2 . If a drawing is referred to, between the common front face of the field electric discharge plasma display panel 1 and the common tooth-back glass substrate 10, and 13 An address electrode line (A1, A2, A3, --, Am-2, Am-1, Am), It has the dielectric layer 11,141, the scanning electrode line (Y1, Y2, --Yn-1, Yn), the common electrode line (X1, X2, --, Xn-1, Xn), and the 1 magnesium-oxide (MgO) layer 12 as a protective layer.
[0003] An address electrode line (A1, A2, A3, --Am-2, Am-1, Am) is applied by the pattern which was fixed in the front face of the tooth-back glass substrate 13. A fluorescent substance 142 is applied to the front face of an address electrode line (A1, A2, A3, --Am-2, Am-1, Am). In addition, when a dielectric layer 141 is applied to the front face of an address electrode line (A1, A2, A3, --Am-2, Am-1, Am), it can apply on the dielectric layer 141.
[0004] A common electrode line (X1, X2, --, Xn-1, Xn) and a scanning electrode line (Y1, Y2, --, Yn-1, Yn) are formed by the pattern which was fixed at the tooth back of the front-windshield substrate 10 so that it might intersect perpendicularly with an address electrode line (A1, A2, A3, --, Am-2, Am-1, Am). Each crossing specifies the ****ing pixel. Each common electrode line (X1, X2, --, Xn-1, Xn) and each scanning electrode line (Y1, Y2, --, Yn-1, Yn) consist of an ITO (Indium Tin Oxide) electrode line (Xna, Yna) and a bus electrode line (Xnb, Ynb) of the metal quality of the material.
[0005] A dielectric layer 11 is applied and formed in the tooth back of a common electrode line (X1, X2, --, Xn-1, Xn) and a scanning electrode line (Y1, Y2, --, Yn-1, Yn). The 1 magnesium-oxide (MgO) layer 12 for protecting a panel 1 from strong electric field is applied and formed in the tooth back of a dielectric layer 11. The gas for plasma formation is sealed by discharge space 14.
[0006] The drive method fundamentally applied to such a plasma display panel is a method with which reset, the address, and a maintenance electric discharge stage are carried out one by one by the unit subfield. In a reset stage, it acts so that the residual wall charge from a subfield may be eliminated. In an address stage, it acts so that a wall charge may be formed in the selected pixel field. And in a maintenance electric discharge stage, it acts so that light may be generated in the pixel in which the wall charge was formed in the address stage.
[0007] That is, if the alternating current pulse of high voltage is impressed relatively between a common electrode line (X1, X2, --, Xn-1, Xn) and a scanning electrode line (Y1, Y2, --, Yn-1, Yn), field electric

discharge will be caused by the pixel in which the wall charge was formed. Under the present circumstances, plasma is formed by discharge space 14, a fluorescent substance 142 is excited by the ultraviolet radiation, and light is generated.

[0008] A desired gradation display is executable with the maintenance charging-time-value width of face of each subfield by containing many unit subfields with the above fundamental principles of operation in a unit frame here.

[0009] As the conventional drive method connected with application of such a drive method, there is the address drive method during the display with the address / the display separation drive method.

[0010] The address / the display separation drive method is the drive methods by which an address period and a maintenance electric discharge period are separated by the unit subfield set up for the gradation display. Thereby, a design and change of a driving gear are easy, and there is an advantage to which a driving gear becomes simple. However, it has the trouble that a maintenance electric discharge period becomes short relatively, and display brightness becomes low.

[0011] On the other hand, the address drive method is the drive method by which mutual superposition is carried out during a display, an address period being contained in the display period of each subfield, and each subfield having unit time difference to each scanning electrode line, and starting one by one. There is an advantage to which a maintenance electric discharge period is relatively prolonged, and display brightness becomes high by this. However, there is a trouble that a design and change of a driving gear are difficult, and a driving gear becomes complicated.

[0012]

[Problem(s) to be Solved by the Invention] The purpose of this invention is to offer the drive method of a plasma display panel that a design and change of a driving gear become easy, a driving gear becomes simple and display brightness also becomes high.

[0013]

[Means for Solving the Problem] The drive method of this invention for attaining the aforementioned purpose It has the front substrate and tooth-back substrate by which mutual opposite isolation was carried out. between the front face of the above, and a tooth-back substrate A common electrode line, A scanning electrode line and an address electrode line align, and the aforementioned common electrode line and a scanning electrode line align by mutual ****. The aforementioned address electrode line aligns to the aforementioned scanning electrode line at a rectangular cross. It is the drive method for carrying out a gradation display by p subfields by which an address stage, a maintenance electric discharge stage, and a reset stage are respectively carried out by the unit frame of the plasma display panel as which the pixel which ****s in each crossing was specified.

[0014] This method includes the stage of dividing the unit frame displayed into the unit drive period of the number which ****s in the number of gradation. each aforementioned unit drive period is divided into three to a unit address period, a unit maintenance electric discharge period, and a unit reset period -- having -- each unit address period -- mutual -- the same -- each unit maintenance electric discharge period -- mutual -- the same -- each unit reset period -- mutual -- it is the same Each aforementioned unit address period is divided at p time, and is assigned to each divided subfield. The mutual superposition of each aforementioned subfield is carried out having the time difference of the aforementioned unit drive period to each aforementioned scanning electrode line, and starting one by one. in each quota **** time in each aforementioned unit address period, address voltage is impressed between the scanning electrode lines and address electrode lines which **** to the unit drive period of the beginning of a subfield Maintenance discharge voltage is impressed between a common electrode line and all scanning electrode lines the unit maintenance electric discharge period of all above. With each aforementioned unit reset period, reset voltage is impressed between the aforementioned common electrode line and the scanning electrode line which ****s to the last unit drive period of a subfield.

[0015] Even if maintenance discharge voltage is impressed between a common electrode line and all scanning electrode lines the unit maintenance electric discharge period of all above, only the pixel in which it was chosen as the address period in front of it, and the wall charge was formed can carry out

maintenance electric discharge.

[0016] As mentioned above, according to the drive method of this invention, it drives with each aforementioned unit drive period, and maintenance discharge voltage is impressed between a common electrode line and all scanning electrode lines the unit maintenance electric discharge period of all above. Thereby, a design and change of a driving gear become easy, and a driving gear may become simple. Moreover, the mutual superposition of each aforementioned subfield is carried out, having the time difference of the aforementioned unit drive period to each aforementioned scanning electrode line, and starting one by one. Thereby, a maintenance electric discharge period is relatively prolonged within a unit frame, and display brightness becomes high.

[0017]

[Embodiments of the Invention] Hereafter, with reference to the appended drawing, the form of desirable operation of this invention is explained in detail.

[0018] Drawing 1 shows the structure of the unit frame for explaining the drive method of the form 1 operation of this invention. The drive method of drawing 1 between a front face and the tooth-back substrates 4 and 13 768 common electrode lines (X1, --, X768), 768 scanning electrode lines (Y1, --, Y768) and address electrode lines (A1, --, Am) align. A common electrode line (X1, --, X768) and a scanning electrode line (Y1, --, Y768) align by mutual ****. An address electrode line (A1, --, Am) aligns to a scanning electrode line (Y1, --, Y768) at a rectangular cross, and it is applied to the plasma display panel as which the pixel which ****s in each crossing was specified. Moreover, it is the drive method for carrying out 256 gradation displays by eight subfields by which an address stage, a maintenance electric discharge stage, and a reset stage are respectively carried out on a unit frame.

[0019] If drawing 1 is referred to, the unit frame displayed will be divided into the unit drive period (H1, --, H255) of 255 pieces fewer [one] than the number of gradation. Each unit drive period (H1, --, H255) is divided into three by a unit address period (Pa1, --, Pa255), a unit maintenance electric discharge period (Ps1, --, Ps255), and the unit reset period (Pr1, --, Pr255). here -- each unit address period (Pa1, --, Pa255) -- mutual -- the same -- each unit maintenance electric discharge period (Ps1, --, Ps255) -- mutual -- the same -- each unit reset period (Pr1, --, Pr255) -- mutual -- it is the same

[0020] The mutual superposition of each subfield is carried out having the time difference of a unit drive period (H1, --, H255) to each scanning electrode line (Y1, --, Y768), and starting one by one. Although the time of the start point in time of each subfield to an end time occupies one frame, since all are superimposed even when each subfield is any, it has the result by which all subfields are included in one frame. The 1st subfield contains a n-th unit drive period to a n-th scanning electrode line. The 2nd subfield contains the n+1st n+2nd unit drive periods to a n-th scanning electrode line. The 3rd subfield contains the n+6th unit drive period from the n+3rd to a n-th scanning electrode line. The 4th subfield contains the n+14th unit drive period from the n+7th to a n-th scanning electrode line. The 5th subfield contains the n+30th unit drive period from the n+15th to a n-th scanning electrode line. The 6th subfield contains the n+62nd unit drive period from the n+31st to a n-th scanning electrode line. The 7th subfield contains the n+126th unit drive period from the n+63rd to a n-th scanning electrode line. And the 8th subfield contains the n+254th unit drive period from the n+127th to a n-th scanning electrode line. Thereby, 256 gradation displays are executable.

[0021] Each unit address period (Pa1, --, Pa255) is divided at eight time (Pas1, --, Pas8) which ****s in the number of subfields, and each divided time (Pas1, --, Pas8) is assigned to each subfield. The 1st hour (Pas1) of each unit address period (Pa1, --, Pa255) to the 1st subfield To the 2nd subfield, the 3rd hour (Pas3) the 2nd hour (Pas2) to the 3rd subfield the 4th hour (Pas4) -- the 4th subfield -- the 5th hour (Pas5) -- the 5th subfield -- it is assigned to the 7th subfield the 7th hour (Pas7), and the 6th hour (Pas6) is respectively assigned to the 6th subfield the 8th hour (Pas8) at the 8th subfield Thus, each unit address period (Pa1, --, Pa255) is because division and the reason assigned are altogether superimposed even when each subfield is any. That is, when different from each other, it is for carrying out addressing and carrying out addressing only of the one pixel for every time.

[0022] in each quota **** time in each unit address period (Pa1, --, Pa255), address voltage is impressed

between the scanning electrode lines (it is any one in Y1, --, Y768) and address electrode lines (it is any one in A1, --, Am) which **** to the unit drive period of the beginning of a subfield Maintenance discharge voltage is impressed between a common electrode line (X1, --, X768) and all scanning electrode lines (Y1, --, Y768) all unit maintenance electric discharge periods (Ps1, --, Ps255). That is, two or more pulses are impressed to a common electrode line (X1, --, X768) and all scanning electrode lines (Y1, --, Y768) by turns. With each unit reset period (Pr1, --, Pr255), reset voltage is impressed between a common electrode line (X1, --, X768) and the scanning electrode line (they are eight lines of the number of subfields in Y1, --, Y768) which ****s to the last unit drive period of a subfield.

[0023] the [for example, / the 1st and] -- it is as follows when the drive process in 2 drive periods (H1, H2) is explained

[0024] Address voltage is impressed between the 1st scanning electrode line (Y1) and the ****ing address electrode line (it is any one in A1, --, Am), and a wall charge is generated by the pixel displayed in the 1st hour (Pas1) in the 1st unit address period (Pa1). Maintenance discharge voltage is impressed the 1st unit maintenance electric discharge period (Ps1) between a common electrode line (X1, --, X768) and all scanning electrode lines (Y1, --, Y768). Maintenance electric discharge is carried out by the pixel displayed by this. With the 1st unit reset period (Pr1), reset voltage is impressed between a common electrode line (X1, --, X768) and eight scanning electrode lines (Y1, Y2, --) which **** to the last unit drive period of a subfield. Thereby, reset electric discharge is carried out by the pixel which ****s at the last time of a subfield.

[0025] Address voltage is impressed between the 1st scanning electrode line (Y1) and the ****ing address electrode line (it is any one in A1, --, Am), and a wall charge is generated by the pixel displayed in the 1st hour (Pas1) in the 2nd unit address period (Pas2). Address voltage is impressed between the 1st scanning electrode line (Y2) and the ****ing address electrode line (it is any one in A1, --, Am), and a wall charge is generated by the pixel displayed in the 2nd hour (Pas2) in the 2nd unit address period (Pa2). Maintenance discharge voltage is impressed the 2nd unit maintenance electric discharge period (Ps2) between a common electrode line (X1, --, X768) and all scanning electrode lines (Y1, --, Y768). Maintenance electric discharge is carried out by the pixel displayed by this. With the 2nd unit reset period (Pr2), reset voltage is impressed between a common electrode line (X1, --, X768) and eight scanning electrode lines (Y2, Y3, --) which **** to the last unit drive period of a subfield. Thereby, reset electric discharge is carried out by the pixel which ****s at the last time of a subfield.

[0026]

[Effect of the Invention] As mentioned above, according to the drive method of the plasma display panel concerning this invention, it drives with each unit drive period (H1, --, H255), and maintenance discharge voltage is impressed to all unit maintenance electric discharge periods (Ps1, --, Ps255) by turns between a common electrode line (X1, --, X768) and all scanning electrode lines (Y1, --, Y768). Thereby, a design and change of a driving gear become easy, and a driving gear may become simple. Moreover, the mutual superposition of each subfield is carried out, having the time difference of a unit drive period (H1, --, H255) to each scanning electrode line (Y1, --, Y768), and starting one by one. Thereby, a maintenance electric discharge period (Ps1+Ps2+--+Ps255) is relatively prolonged within a unit frame, and display brightness may become high.

[0027] this invention can be transformed and improved by this contractor by the thought of invention defined by not only the gestalt of the aforementioned implementation but the claim, and within the limits.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is structural drawing of the unit frame for explaining the drive method of the gestalt 1 operation of this invention.
[Drawing 2] It is the drawing in which the structure of a general plasma display panel is shown.
[Drawing 3] It is the electrode line pattern view of the plasma display panel of drawing 2 .
[Drawing 4] It is the cross section showing the example of further others of one pixel of the panel of drawing 2 .
[Description of Notations]
1 Display Panel
10 13 Glass substrate
11,141 Dielectric layer
12 1 Magnesium-Oxide Layer
14 Discharge Space
142 Fluorescent Substance

[Translation done.]